Amendments to the Specification:

Please replace the paragraphs between page 3, line 17, and page 4, line 12, with the following amended paragraphs:

~~Fig. 10(A) shows~~ Figs. 10(A), 10(C) and 10(D) show an example where the level shifter 905 shown in Fig. 9 is constituted by a conventional level shifter. When voltage amplitude of the input signals (In, Inb) is as small as about 3.3 V, the level shifter having such a construction sometimes fails to normally conduct level conversion owing to influences of the threshold values of the TFT constituting the level shifter.

Therefore, a level shifter having a construction shown in ~~Fig. 10(B)~~ Figs. 10(B) and 10(E) to 10(H) is employed. The level shifter shown in ~~Fig. 10(B)~~ Figs. 10(B) and 10(E) to 10(H) conducts level conversion by means of a differential amplifier, and can accomplish a reliable level conversion function even when voltage amplitude of the input signals is small. Therefore, this is an extremely effective circuit for achieving low voltage driving of the circuit. The level shifter using the differential amplifier is disclosed in Japanese Patent Application No. 2000-193498.

On the other hand, the level shifter shown in ~~Fig. 10(B)~~ Figs. 10(B) and 10(E) to 10(H) needs a current source. In other words, since a constant current is always supplied during driving of the circuit (regardless of driving or stop of the level shifter), this current impedes low power consumption of the display device as a whole.

Please replace the paragraph beginning at page 15, line 2, with the following amended paragraph:

~~Fig. 2 is~~ Figs. 2(A) to 2(E) show a circuit diagram of a level shifter and a current source;

Please replace the paragraph beginning at page 15, line 20, with the following amended paragraph:

Figs. 10(A) ~~and 10(B)~~ to 10(H) are circuit diagrams of level shifters and current sources;

Please replace the paragraph beginning at page 16, line 9, with the following amended paragraph:

~~Fig. 17 shows~~ Figs. 17(A) to 17(C) show an example of a shift register using a D flip-flop.

Please replace the paragraph beginning at page 17, line 4, with the following amended paragraph:

The level shifter current source 105 and the level shifter 106 have the construction shown in ~~Fig. 2~~ Figs. 2(A) to 2(E). The level shifter is of the type that executes level conversion of signals by utilizing a differential amplifier in the same way as the level shifter used in the source signal line driving circuit shown in Fig. 9. The level shifter current source 105 corresponds to a block indicated by reference numeral 201 in ~~Fig. 2~~ Figs. 2(A) to 2(E). Only when a pulse is inputted to an input terminal 31, TFT 203 and 204 become conductive and the current source 105 can supply a current to each level shifter.

Please replace the paragraphs between page 23, line 4, and page 24, line 9, with the following amended paragraphs:

The shift register of the driving circuit of the embodiment shown in Fig. 6 uses an ordinary type such as a D flip-flop (D-FF) type shown in ~~Fig. 17(A)~~ Figs. 17(A) and 10(C). This D-FF holds the potential of the input terminal at the fall timing of the clock signal (CK) and remains under the holding state till the fall of the next clock signal. Therefore, the input/output becomes such as shown in Fig. 17(B). The output pulses have a pulse width twice that of the clock signal and are serially outputted. Each pulse overlaps with one another at its 1/2 pulse width.

The shift register output inputted to the NAND circuit overlaps with the pulses of the adjacent stages as shown in the timing chart of Fig. 8(A). This has already been described with reference to ~~Fig. 17(A)~~ Figs. 17(A) to 17(C). The period in which the LS power source 1 is ON is the period from the timing at which the shift register of the first stage in the first unit outputs the pulse to the timing at which the pulse output from the shift register of the kth stage terminates. When the shift register of the k+1th stage of the subsequent second unit outputs the pulse, the LS power source 2 is turned ON. Here, since the output pulse of the shift register of the kth stage overlaps with the output pulse of the shift register of the k+1th stage, a period can be provided in which both LS power source 1 and LS power source 2 are kept ON. In other words, since the pulse of the final stage of ath unit (a: natural number, $1 \leq a \leq x$) overlaps with the pulse of the initial stage of the a+1th unit, the current source of the ath unit and the current source of the a+1th unit supply the current during this period. In this way, the supply of the current can be made normally during the level conversion at the timing bridging each unit due to the delay of the pulse, etc, described above.